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PATENT
Docket No.: HEUR-019

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: 2171

Examiner: Not Yet Assigned

Serial No.: 10/055,086

Filed: January 22, 2002

In re Application of: Arman Sagatelian

For: METHOD AND APPARATUS FOR IDENTIFYING CLUSTERS OF FAIL
BITS IN A BITMAP

Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail, in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on August 26, 2003, Signed Cathie Rossman
Cathie Rossman

TRANSMITTAL LETTER

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RECEIVED

SEP 05 2003

Technology Center 2100

Sir:

Enclosed please find the following:

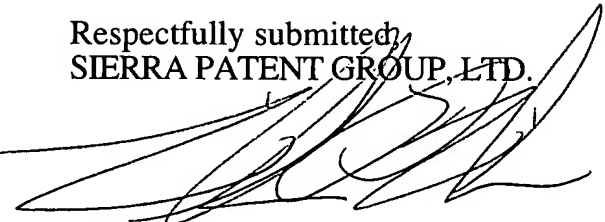
1. Information Disclosure Statement
2. Form PTO-1449
3. Copies of 4 References

In the event any additional fee is required for filing the above-noted document, including any fees required under 37 CFR 1.136 for any necessary Extension of Time to make the filing of attached document timely, the Assistant Commissioner is hereby authorized to charge the fee to our Deposit Account No.: 50-0612.

Dated: 26 Aug 2003

Sierra Patent Group, Ltd.
P.O. Box 6149
Stateline, NV 89449
(775) 586-9500

Respectfully submitted,
SIERRA PATENT GROUP, LTD.


William P. Wilbar
Reg. No.: 43,265



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INFORMATION DISCLOSURE STATEMENT RECEIVED

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SEP 05 2003
Technology Center 2100

Dear Sir:

Each item of information listed in the attached FORM PTO-1449, for which a copy of each is attached, may be material to the examination of the above-identified application and is, therefore, submitted in compliance with the duty of disclosure defined in 37 CFR §§1.56, 1.97 and 1.98. The Examiner is requested to make these items of official record in this application.

This Information Disclosure Statement under 37 CFR §§1.56, 1.97 and 1.98 is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that any one or more of these items constitutes prior art.

I

This statement is filed pursuant to:

(X) 37 C.F.R. §1.97(b).

This information disclosure statement is filed either (1) within three months of the filing date of the national applications; (2) within three months of the date of entry of the national stage as set forth in 37 C.F.R. §1.491 in an international application; or (3) before the mailing date of a first office action on the merits, whichever event occurs last.

Accordingly, this information disclosure statement requires no fee and no certification.

() 37 C.F.R. §1.97(c).

This information disclosure statement is filed after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of either (1) a final action under 37 C.F.R. §1.113 or (2) a notice of allowance under 37 C.F.R. §1.311.

Accordingly, this information disclosure statement requires either the fee specified in 37 C.F.R. § 1.17 (p) or a statement according to 37 C.F.R. §1.97(e).

() 37 C.F.R. §1.97(d).

This information disclosure statement is filed after the period specified in 37 C.F.R. §1.97(c) and filed on or before the payment of the issue fee and is accompanied by

- (1) The statement specified in paragraph (e) of this section; and
- (2) The fee set forth in §1.17(p).

Accordingly, this information disclosure statement requires the fee specified in 37 C.F.R. §1.17(p), \$180.00, for submission of an information disclosure statement under 37 C.F.R. §1.97(d).

37 C.F.R. §1.97(e).

- () (1) Each item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the statement.

- () (2) No item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, or, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. §1.56(c), more than three months prior to the filing of the statement.

If this statement crosses in the mail with an office action, or is otherwise not in the indicated category of 37 C.F.R. §1.97, it is respectfully requested that this statement be treated in the next appropriate category and made of record. To the extent required, please treat this paper as a conditional petition for acceptance of the information disclosure statement.

II


(X) No fee is due.

() The fee specified in 37 C.F.R. §1.17(p) for submission of an information disclosure statement under 37 C.F.R. §1.97(c) or 37 C.F.R § 1.97(d) is enclosed, \$180.00.

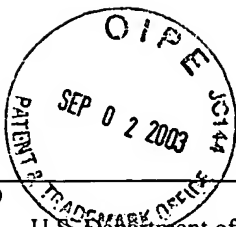
In the event any fee is required for filing the above-noted document, including any fees required under 37 CFR 1.136 for any necessary Extension of Time to make the filing attached document timely, the Assistant Commissioner is hereby authorized to charge the fee to our Deposit Account No. 50-0612. A duplicate of this page is enclosed.

Respectfully submitted,
SIERRA PATENT GROUP, LTD.

Dated: 26 Aug 2003


William P. Wilbar
Reg. No.: 43,265

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(775) 586-9550 Fax



Form PTO 1449 (Rev. 2-32)				U.S. Department of Commerce Patent and Trademark Office		Atty. Docket No. HEUR-019		Serial No. 10/055,086	
Information Disclosure Statement by Applicant						Applicant: Arman Sagatelian			
(Use several sheets if necessary)						Filed: January 22, 2002 Group: 2171			
U.S. Patent Documents									
Init.		Document No.	Date	Name	Class	Subclass	Filing Date		
	1	5,475,695	12/12/1995	Caywood et al.	371	27	03/19/1993		
Foreign Documents									
								Translation	
Init.		Document No.	Date	Country	Class	Subclass	Yes	No	
Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)									
	2	K. Tobin, "Automated Analysis for Rapid Defect Sourcing and Yield Learning", <u>Future Fab International</u> , 15 pages, Vol. 4, 1997 (no month).							
	3	"Semiconductor Spatial Signature Analysis (SSA)", [Internet] http://www-ismv.icornl.gov/projects/SSA.html , 6 pages, Revised March 31, 1999, printed 2/27/03							
	4	J. Segal et al., "The Value of Electrical Bitmap Results from Embedded Memory Arrays for Rapid Yield Learning", Digest of Papers, 2 nd IEEE Latin American Test Workshop LATW2001, pp. 266-272, Feb. 2001.							
Examiner					Date Considered				
Examiner: Initial if citation considered, whether or not citation is in conference with MPEP 609; Draw line through citation if not conformance and not considered. Include a copy of this form with the next communication to applicant.									